



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: V. Markovich et al

Group Art Unit: : Endicott Interconnect Technologies, Inc.
Examiner: : IP Law, FBU/257-4 AA14
Serial No.: : 1701 North Street
Filed: Herewith : Endicott, New York 13760
Title: Stacked Chip Electronic Package Having
Laminate Carrier And Method Of Making Same

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT/CERTIFICATION

For ensuring compliance with Applicant's/Applicants' duty of disclosure under 37 CFR § 1.56, the undersigned hereby submits the documents listed on the attached Form PTO-1449 for consideration by the Examiner in charge of the above-identified patent application.

The listing of these documents is not to be construed as an admission that such is actually prior art with respect to the invention of the present application and is not to be construed that such is material with respect to the present invention.

[] U.S. patent applications which Applicant/Applicants considers/consider to be related to the above-identified application.



- [] A concise explanation of the relevance of the non-English language documents is attached:
- [] The relevance of the documents is indicated on the enclosed copy of the _____ Search Report for the priority application _____.

These documents are being submitted (check only one of the next four boxes):

- [X] within three months of the filing of the above U.S. national application or of the date of entry of the U.S. national stage in an International Patent Application (no fee is due);
- [] before receiving a first Office Action on the merits of the above-identified patent application (no fee is due);
- [] following receipt of a first Office Action, but before issuance of a Final Office Action or a Notice of Allowance (if this box is checked, the fee box below or one of the last two boxes must be checked);

OR

- [] following receipt of a Notice of Allowance or a Final Office Action (if this box is checked, the fee box and one of the last two boxes also must be checked).



CERTIFICATION

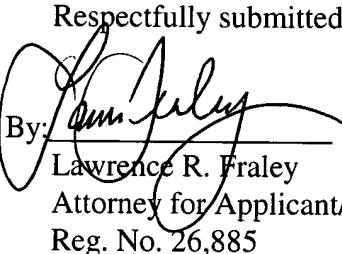
- [] The undersigned certifies that each item of this information is being submitted within three months of the date it was first cited in any communication from a foreign patent office in a counterpart foreign application.

- [] The undersigned certifies that no item of information contained in the information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

Dated: Sept. 11, 2003
Telephone: 607-755-3207
Fax: 607-757-1156

Respectfully submitted,

By:


Lawrence R. Fraley
Attorney for Applicant/Applicants
Reg. No. 26,885

FORM PTO 1449 (Modified)

LIST OF PATENTS AND
PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENTPage 1 of 4

ATTY. DOCKET NO.	EI-2-03-001-CIP-3	SERIAL NO.	N/A
APPLICANT	V. MARKOVICH ET AL		
FILING DATE	HEREWITH	GROUP	N/A

REFERENCE DESIGNATION

U. S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	AA	4,882,454	11/89	Peterson et al			
	AB	4,902,610	02/90	Shipley			
	AC	5,072,075	12/91	Lee et al			
	AD	5,121,190	06/92	Hsiao et al			
	AE	5,336,855	08/94	Kahlert et al			
	AF	5,418,690	05/95	Conn et al			
	AG	5,483,421	01/96	Gedney et al			
	AH	5,574,630	11/96	Kresge et al			
	AI	5,615,087	03/97	Wieloch			
	AJ	5,661,089	08/97	Wilson			
	AK	5,768,109	06/98	Gulick et al			
	AL	5,798,563	08/98	Feilchenfeld et al			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	AM	1-307294	12/1989	Japan (Patent Abstracts of Japan)			
	AN	4025155A2	01/1992	Japan (Patent Abstracts of Japan)			
	AO	6112271A2	04/1994	Japan (Delphion)			
	AP	9-232376	09/1997	Japan (Patent Abstracts of Japan)			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance AND not considered. Include copy of this form with next communication to applicant.

EXAMINER

DATE CONSIDERED

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U. S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	AA	5,838,063	11/98	Sylvester			
	AB	5,891,869	04/99	Lociuro et al			
	AC	5,894,173	04/99	Jacobs et al			
	AD	5,894,517	04/99	Hutchison et al			
	AE	5,900,675	05/99	Appelt et al			
	AF	5,926,377	07/99	Nakao et al			
	AG	5,982,630	11/99	Bhatia			
	AH	6,023,211	02/00	Somei			
	AI	6,075,423	06/00	Saunders			
	AJ	6,081,430	06/00	La Rue			
	AK	6,146,202	11/00	Ramey et al			
	AL	6,222,740 B1	04/01	Bovensiepen et al			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	AM	10-209347	08/98	Japan (Patent Abstracts of Japan)			
	AN	11-087560	03/99	Japan (Patent Abstracts of Japan)			
	AO	2000-022071	01/00	Japan (Patent Abstracts of Japan)			
	AP	2000-024150	01/00	Japan (Patent Abstracts of Japan)			

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APPLICANT

V. MARKOVICH ET AL

FILING DATE

HEREWITH

GROUP

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REFERENCE DESIGNATION

U. S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
AA	6,246,010 B1	06/01	Zenner et al			
AB	6,351,393 B1	02/02	Kresge et al			
AC	6,370,012 B1	04/02	Adae-Amoakoh et al			
AD	6,431,914 B1	08/02	Billman			
AE	6,495,772 B2	12/02	Anstrom et al			
AF	2002/0125967 A1	09/02	Garrett et al			
AG						
AH						
AI						
AJ						
AK						
AL						

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EXAMINER

DATE CONSIDERED

REFERENCE DESIGNATION

OTHER ART

EXAMINER INITIALS		BIBLIOGRAPHIC DATA (Author, Title, Date, Pertinent Pages, etc.)
	AR	IBM TDB, "Multi Chip Cooling Plate", 07/78 pp. 745-746
	AS	IBM TDB, "Simultaneous Chip Placement - Multi-Chip Modules", 02/82 pp. 4647-4649
	AT	IBM TDB, "High Performance Multi-Chip Module", 11/87 pp 437-439
	AU	IBM TDB, "Low-Cost, High-Power, Multi-Chip Module Design", 08/88 pp. 451-452
	AV	IBM TDB, "Thermally Conductive Substrate Mounted Multi-Chip Module Cap", 09/93 pp. 623-624

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